Introduction To The AVSBus

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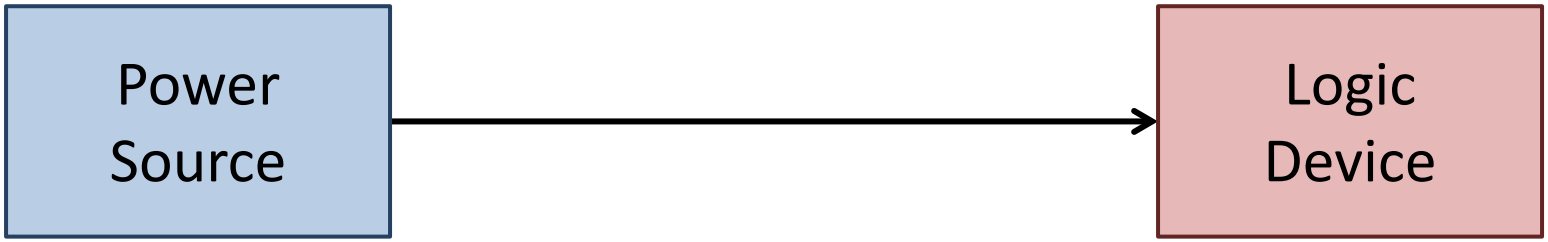
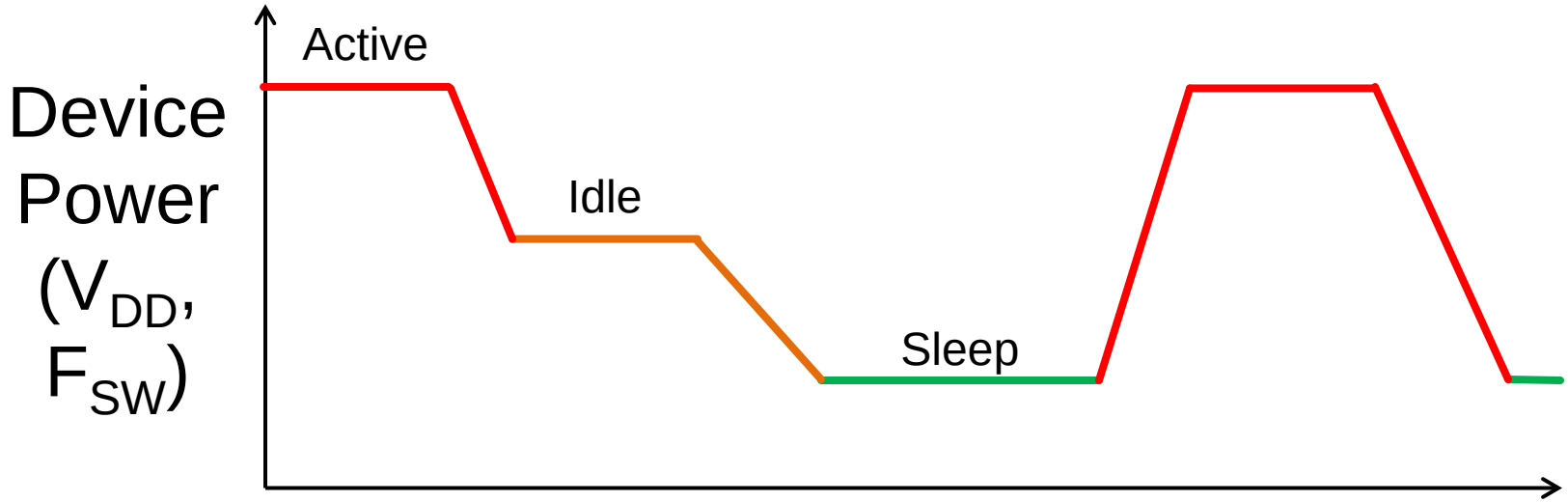
Presentation Overview

- The Need For Speed
- AVSBus Interface And Configurations
- AVS Frames
- AVSBus Commands And Data Format

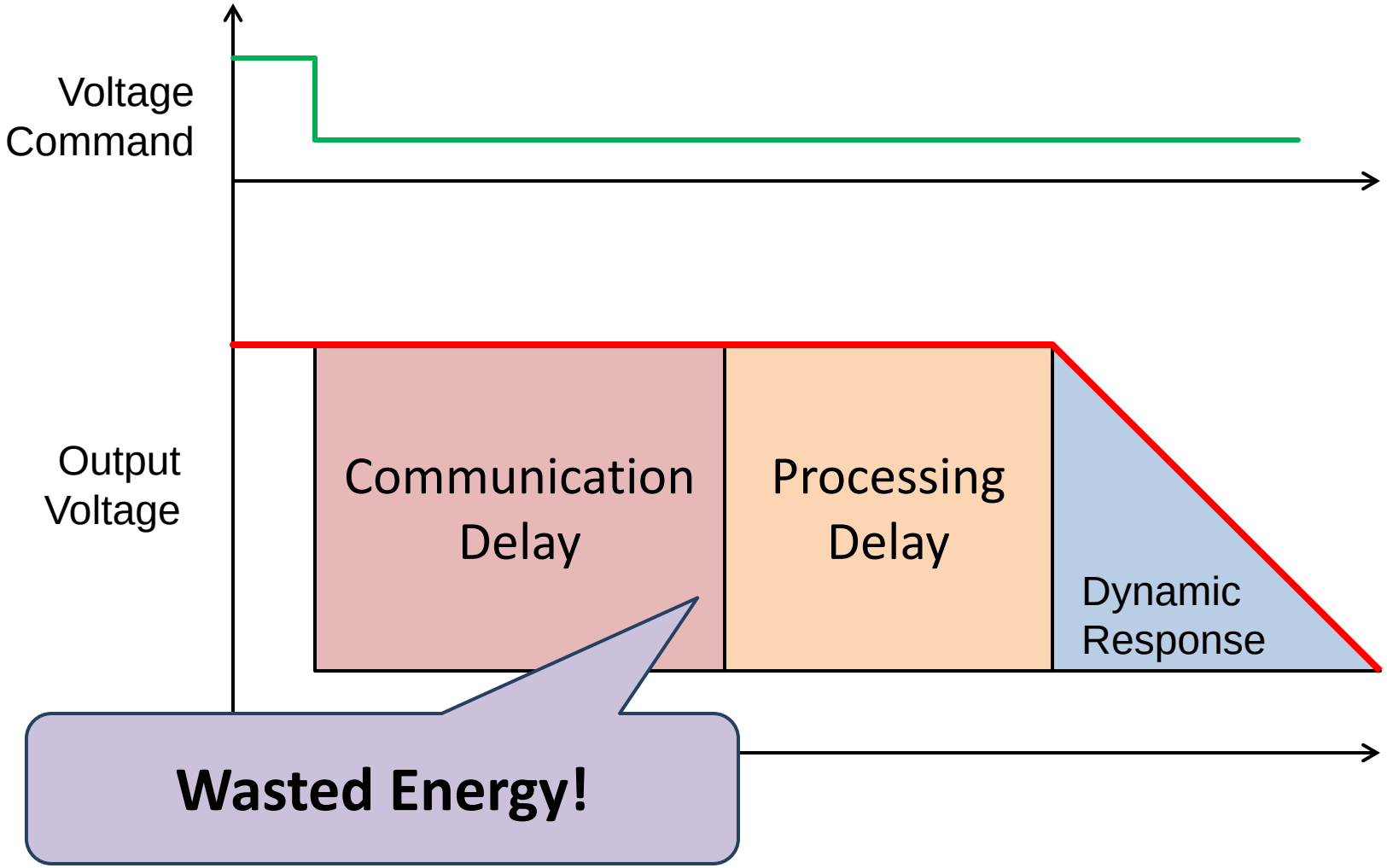
Minimizing Energy Use



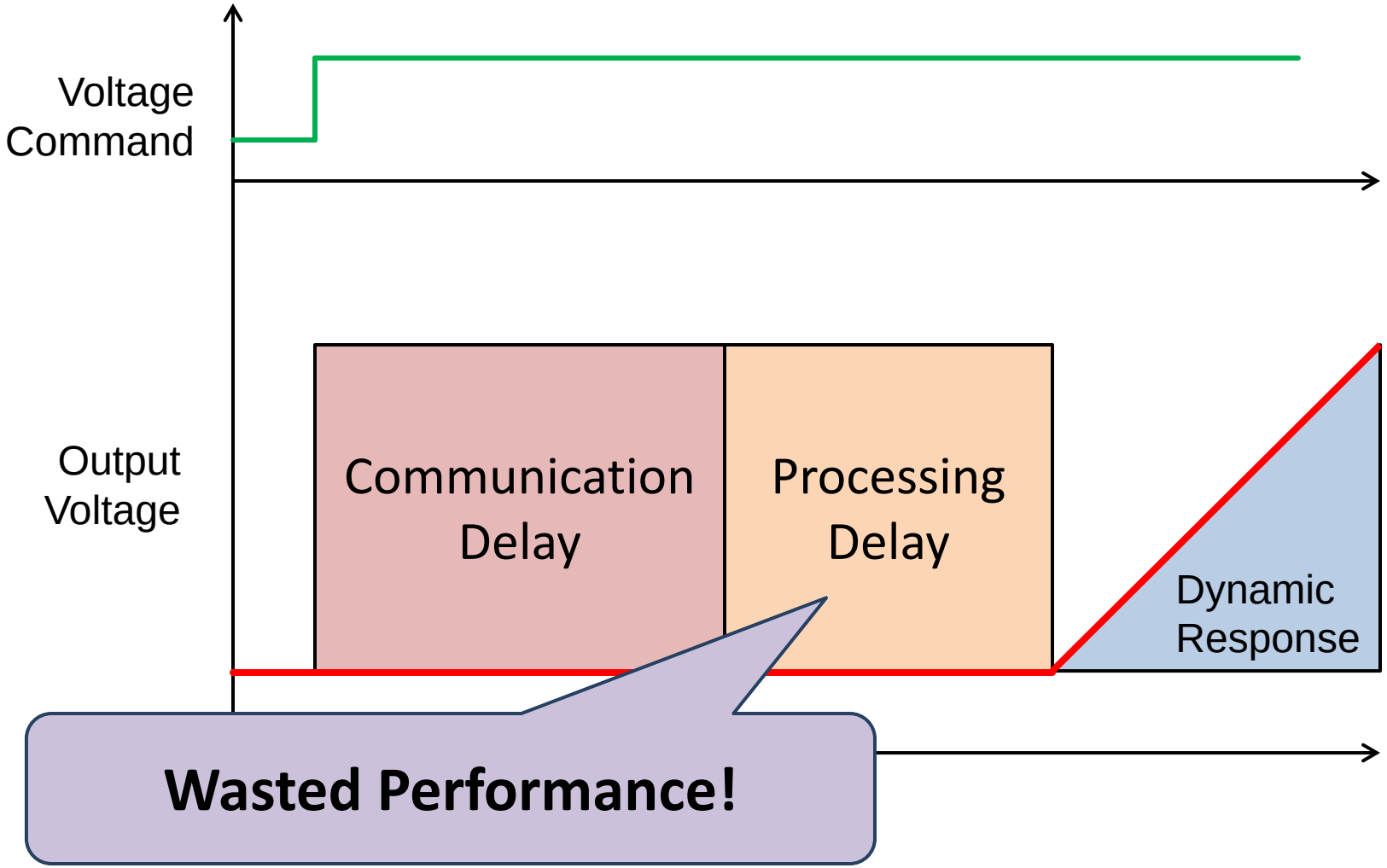
$$P \propto K_{SWITCH} \cdot V_{DD}{}^{2} \cdot F_{SW} + K_{STATIC} \cdot V_{DD}$$



Effect Of Delay



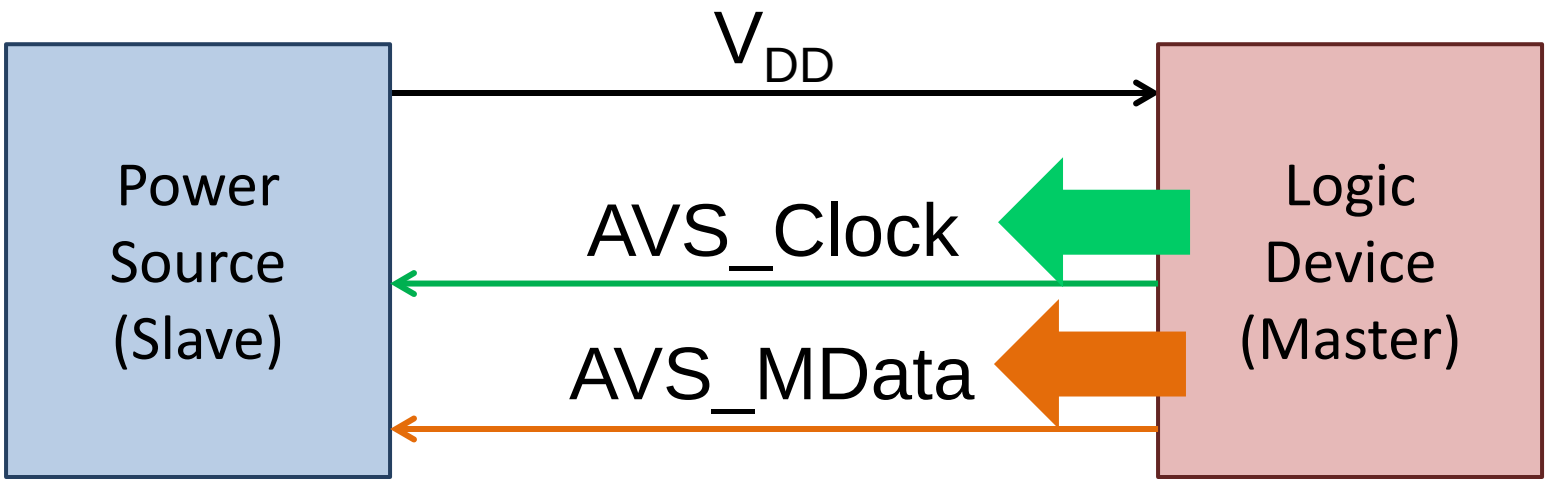
Effect Of Delay



How Much Delay?

- Standard PMBus™ Command: 36 Bits
  - Address: 8 Bits + ACK
  - Command Code: 8 Bits + ACK
  - Voltage Data: 16 Bits + 2 ACKs
- 360 µs @ F_{CLOCK} = 100 kHz
  - 36 µs @ F_{CLOCK} = 1 MHz
- Processing Delay Implementation Dependent
  - Few µs ⇨Tens Of µs

AVSBus

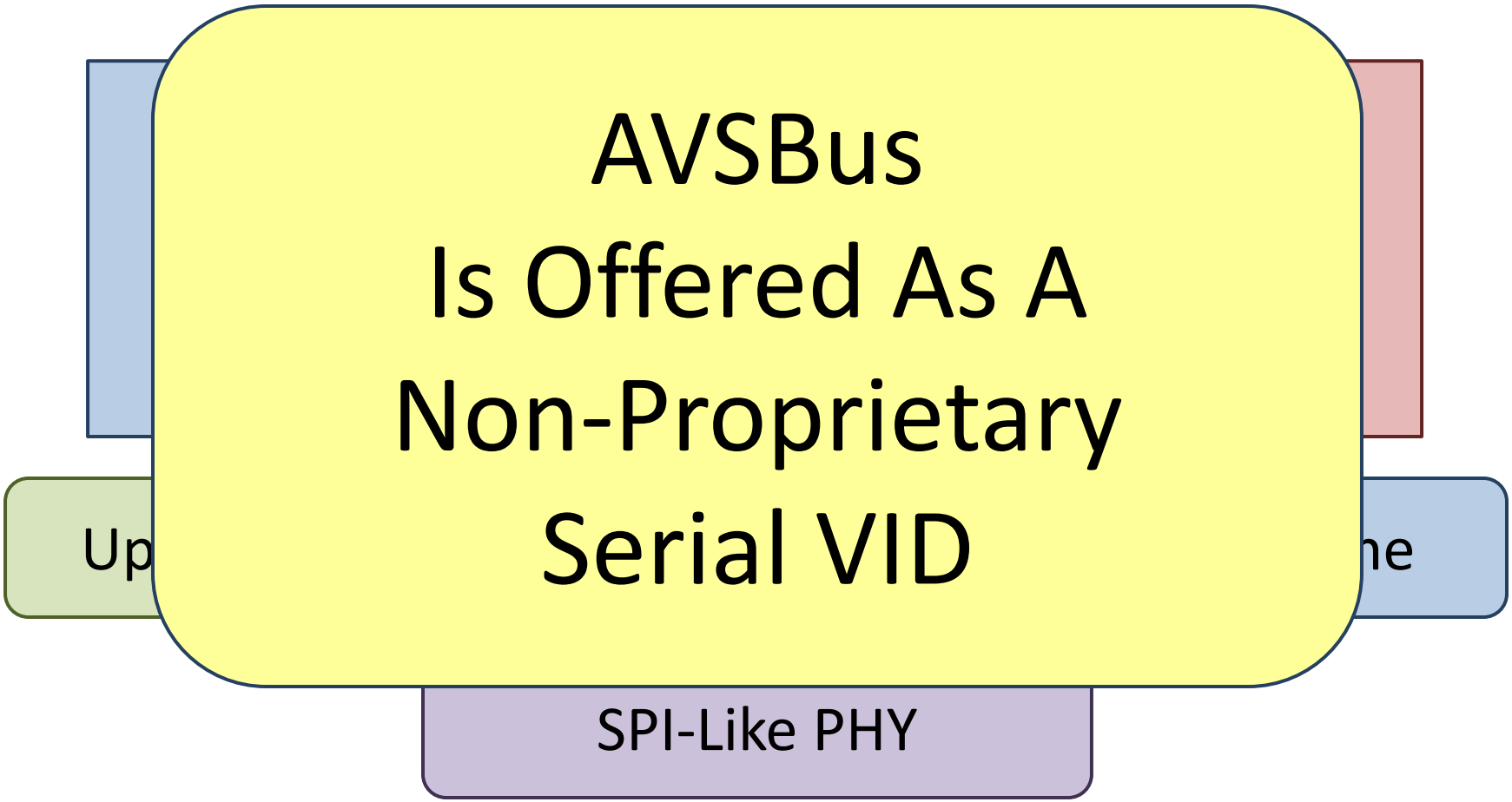


Up to 50 MHz Clock

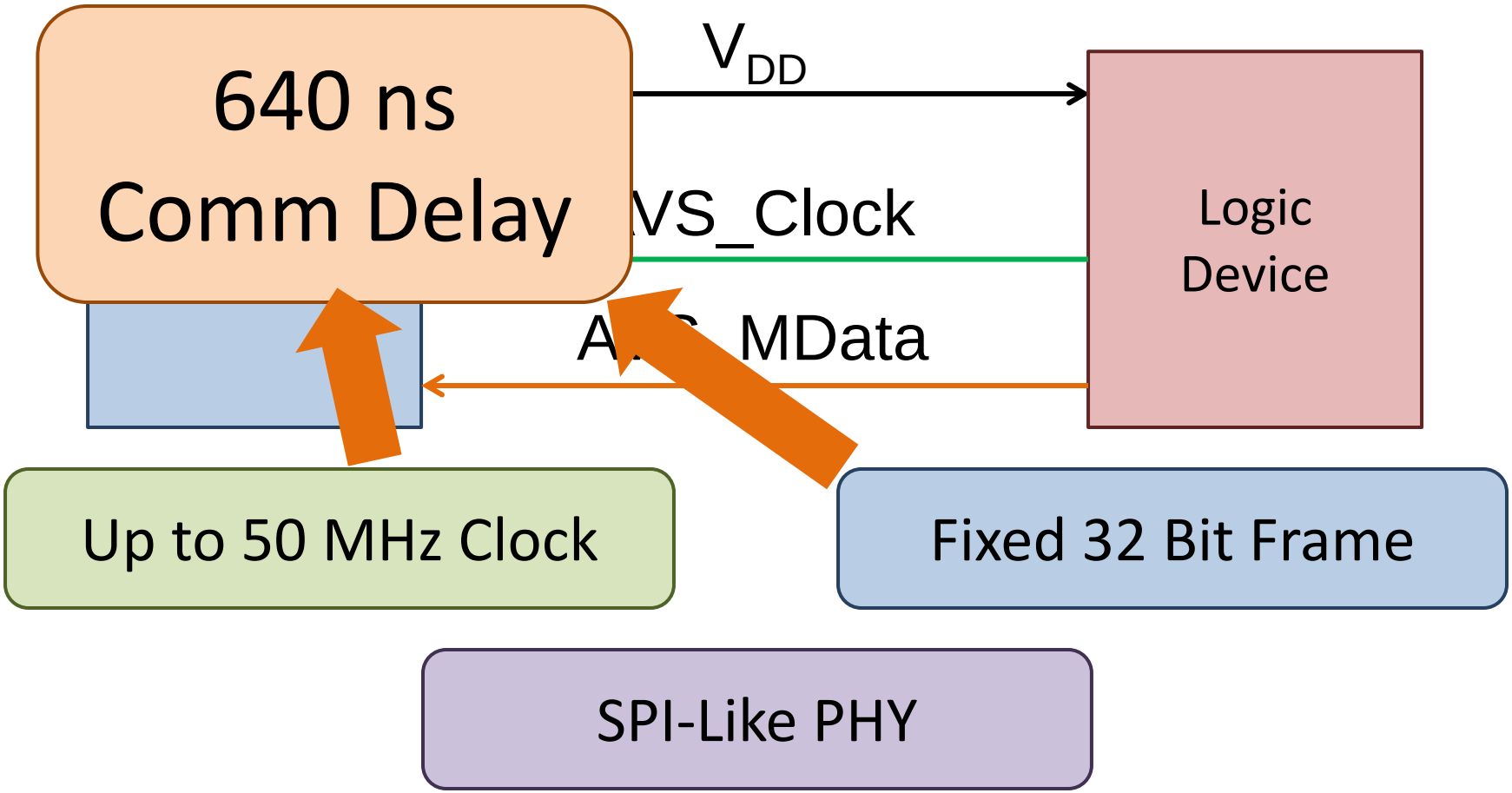
Fixed 32 Bit Frame

SPI-Like PHY

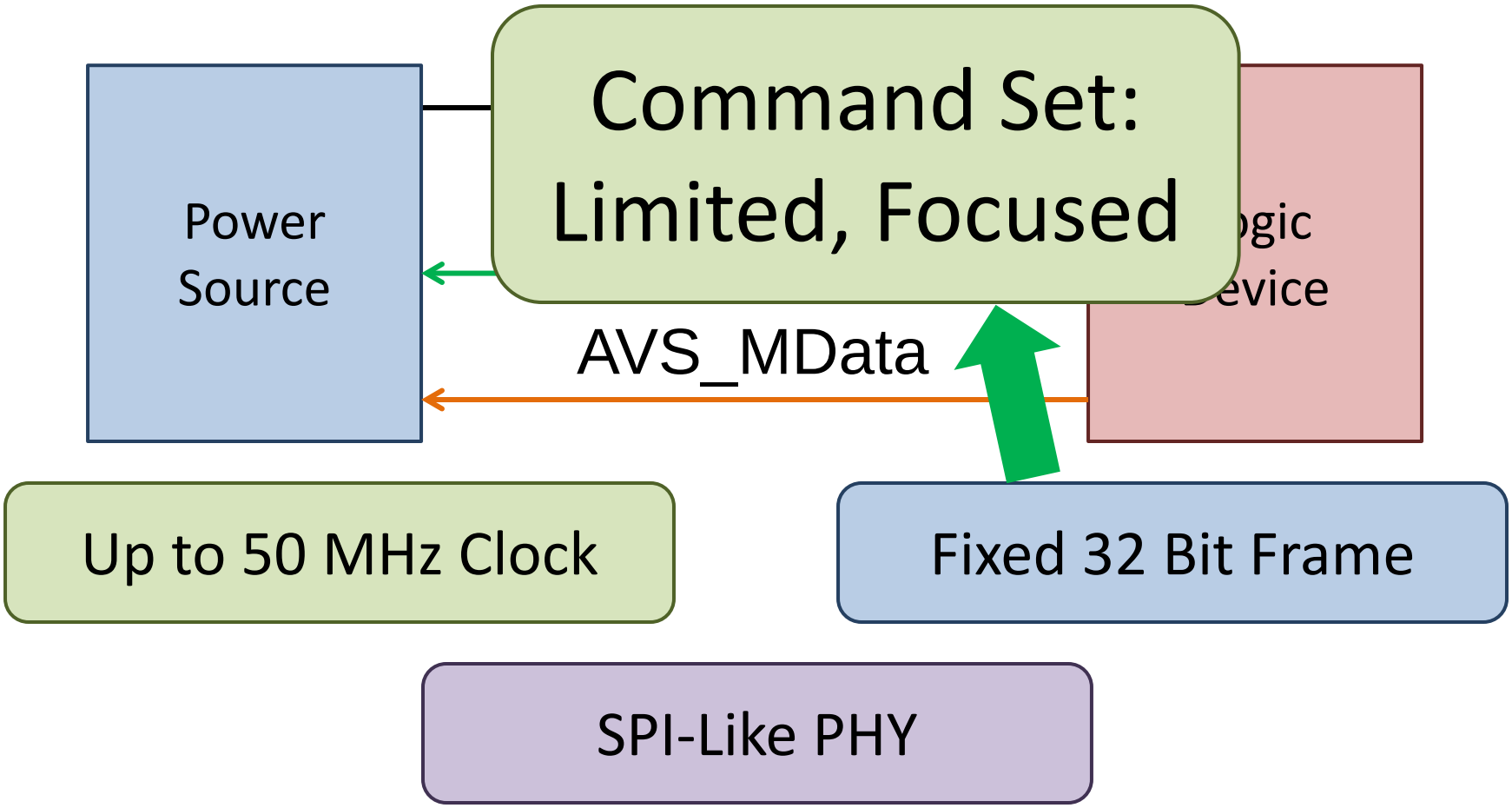
AVSBus



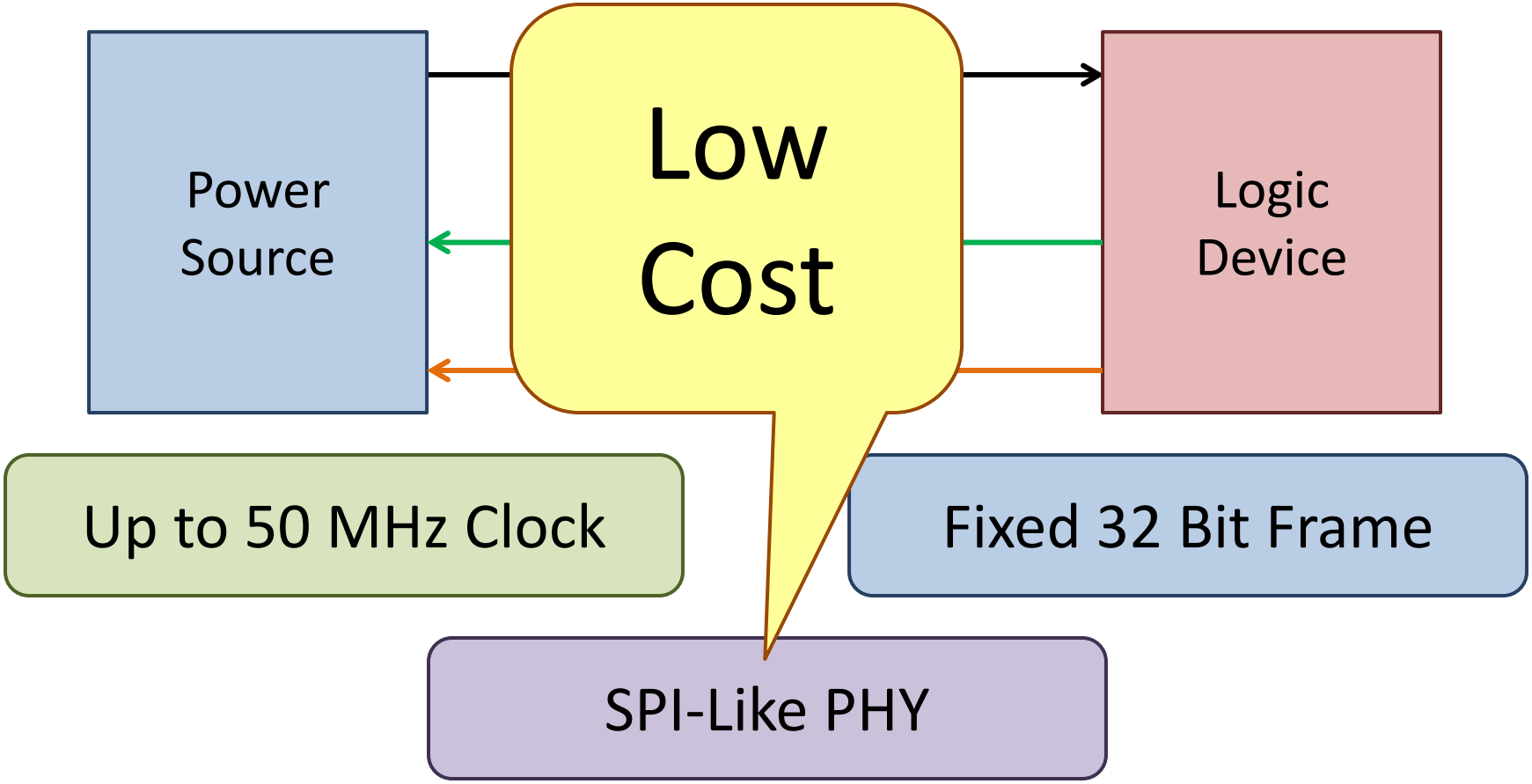
AVSBus



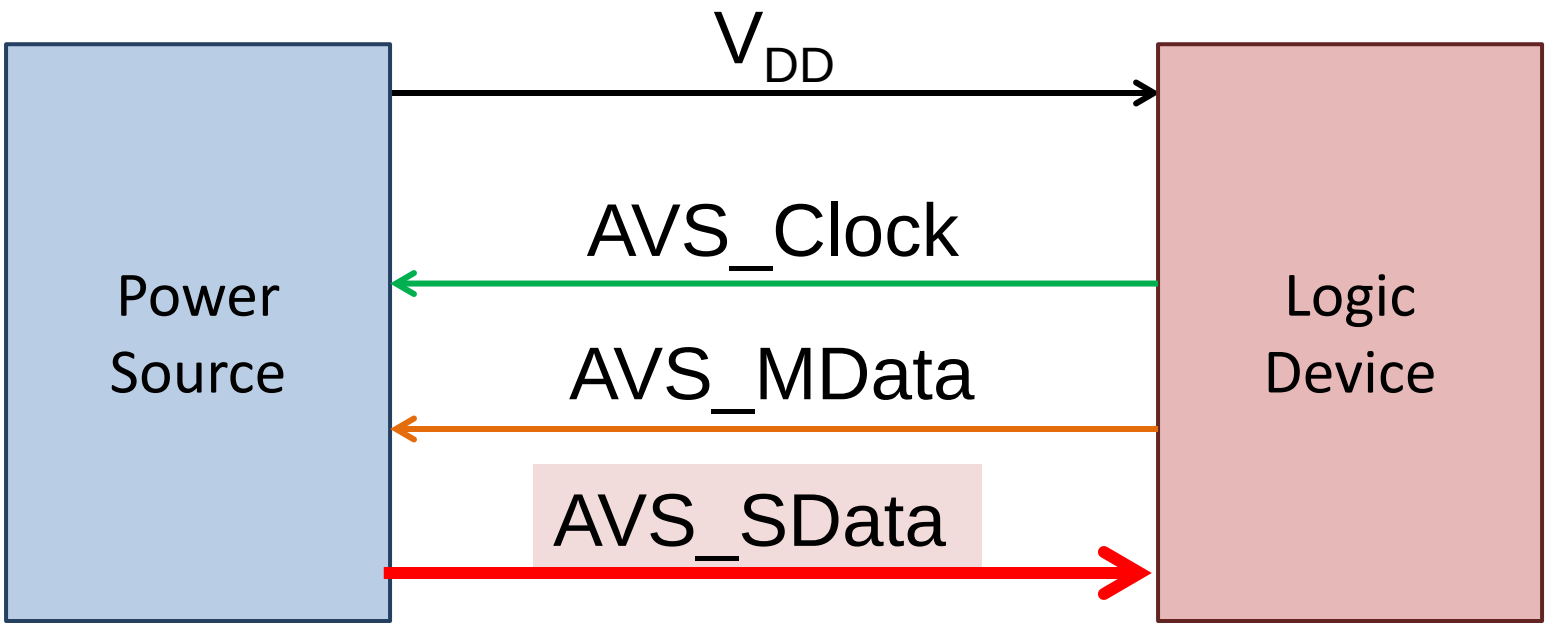
AVSBus



AVSBus

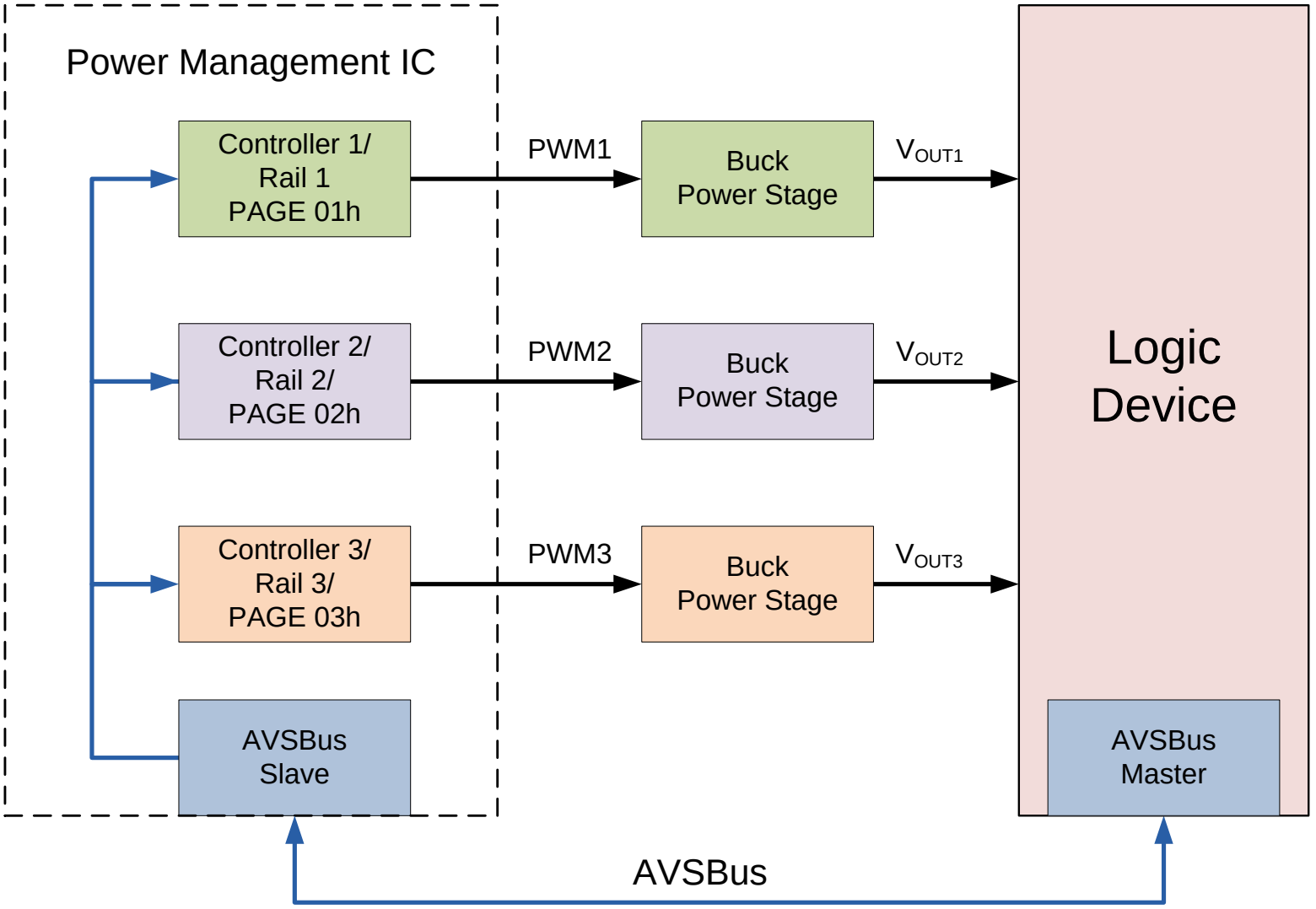


AVSBus 3-Wire Mode

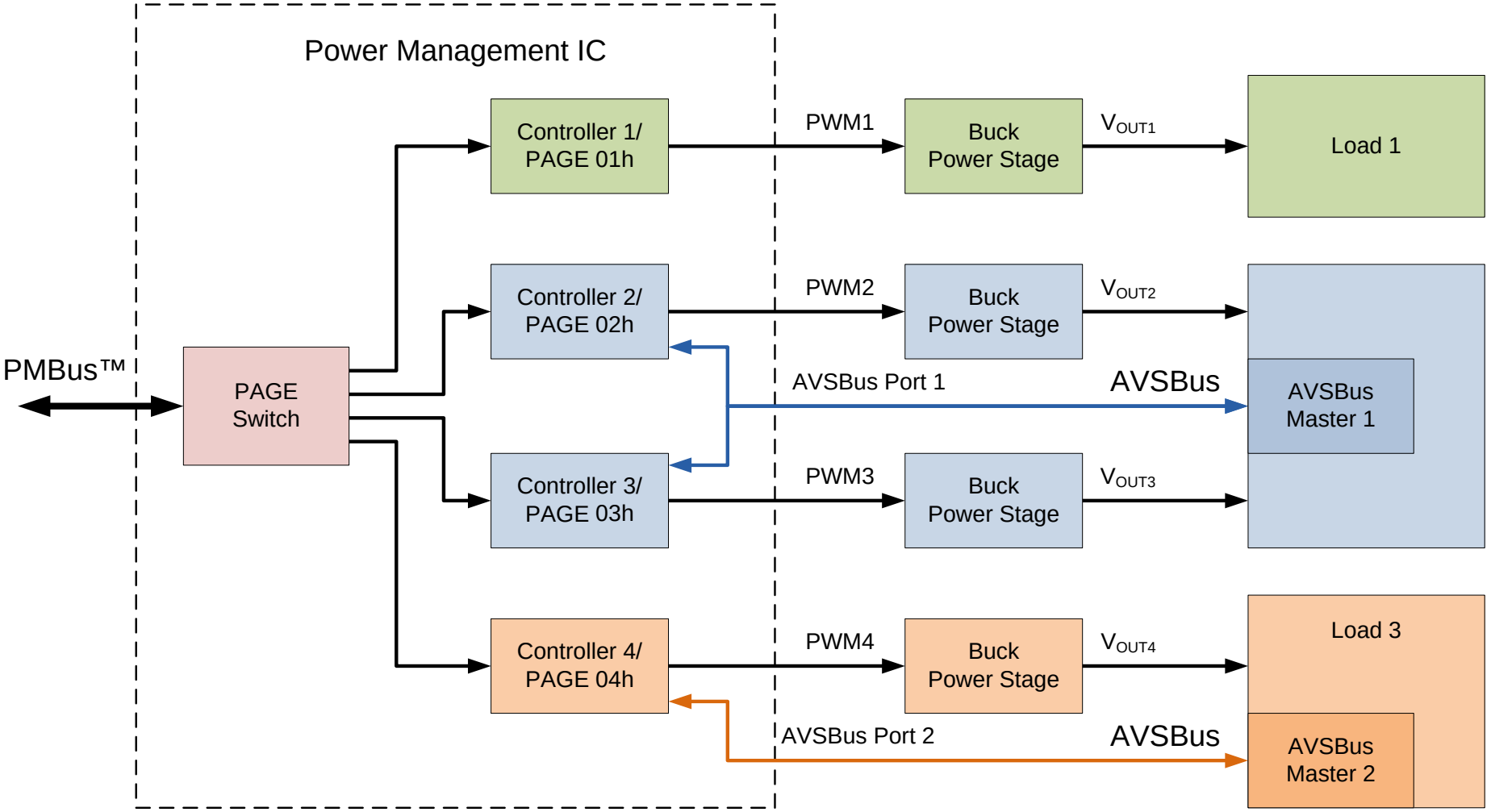


Allows Slaves To Respond To Requests For Status

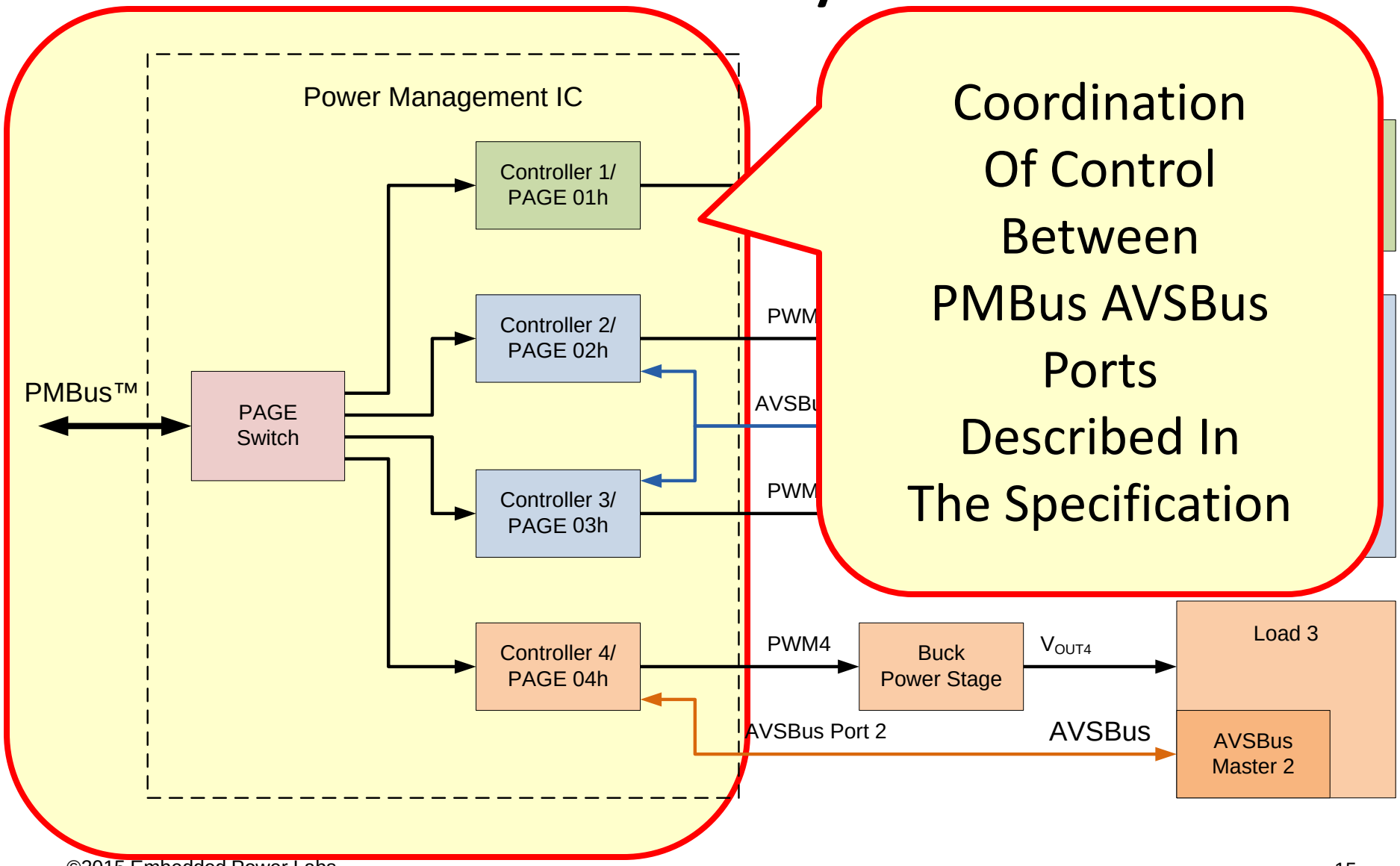
Multi-Rail Devices



Multi-Bus System



Multi-Bus System



Some Basic Rules

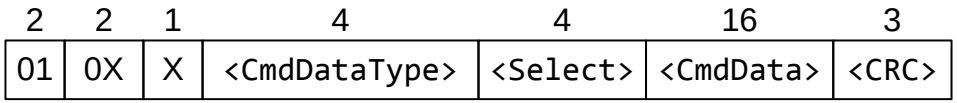
- Data Launch On Clock Rising Edge,
  Data Capture On Clock Falling Edge
- Numeric Data In Two's Complement
- AVS_MDATA 1 To 0 Transition
  Starts A New Frame
- Two Bit Slave ACK
- Every Frame Start Requires A Status Response
- CRC Used For All Frames
- Write And Hold/Write And Commit

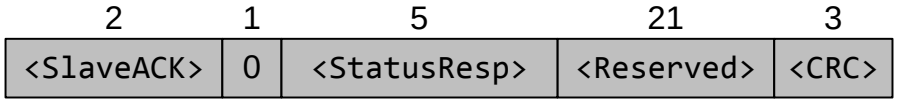
The Write Frame

Frame From Master To Slave

2	2	1	4	4	16	3
01	0X	X	<CmdDataType>	<Select>	<CmdData>	<CRC>

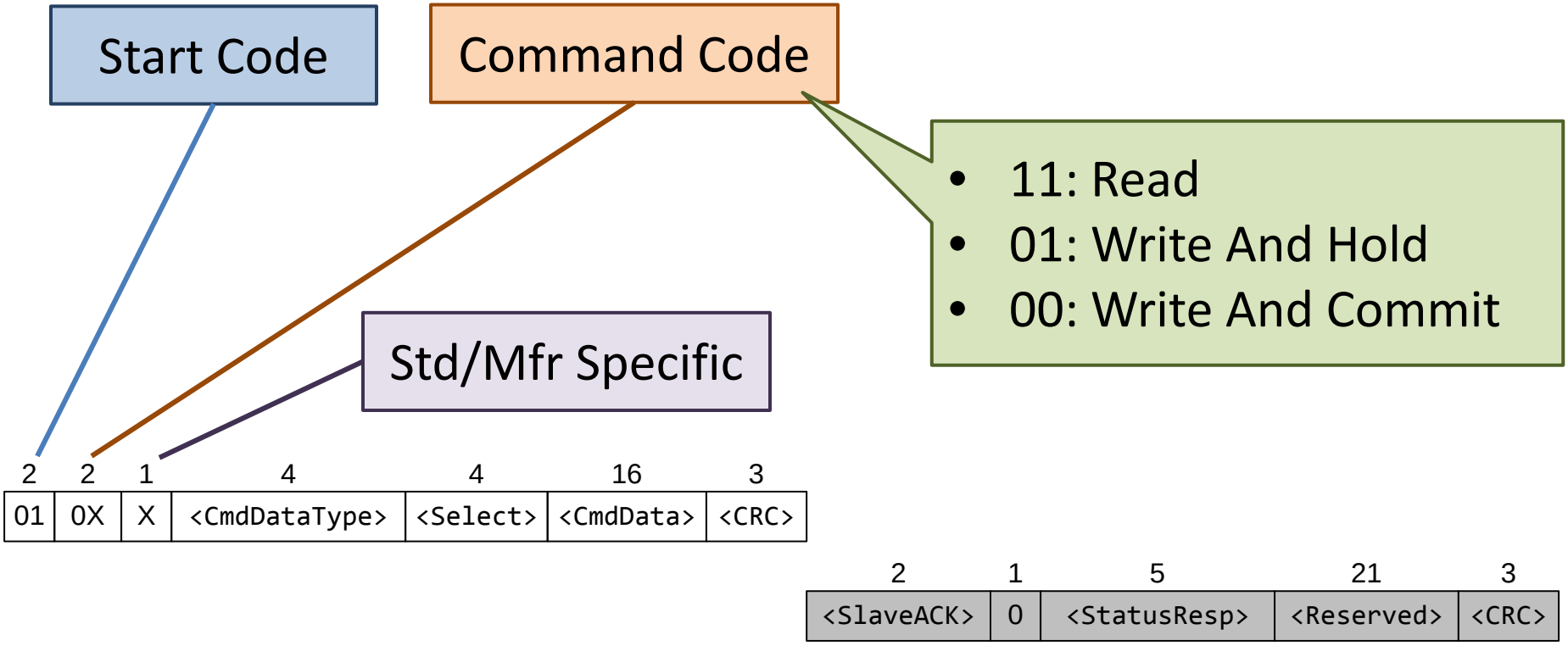
The Write Frame



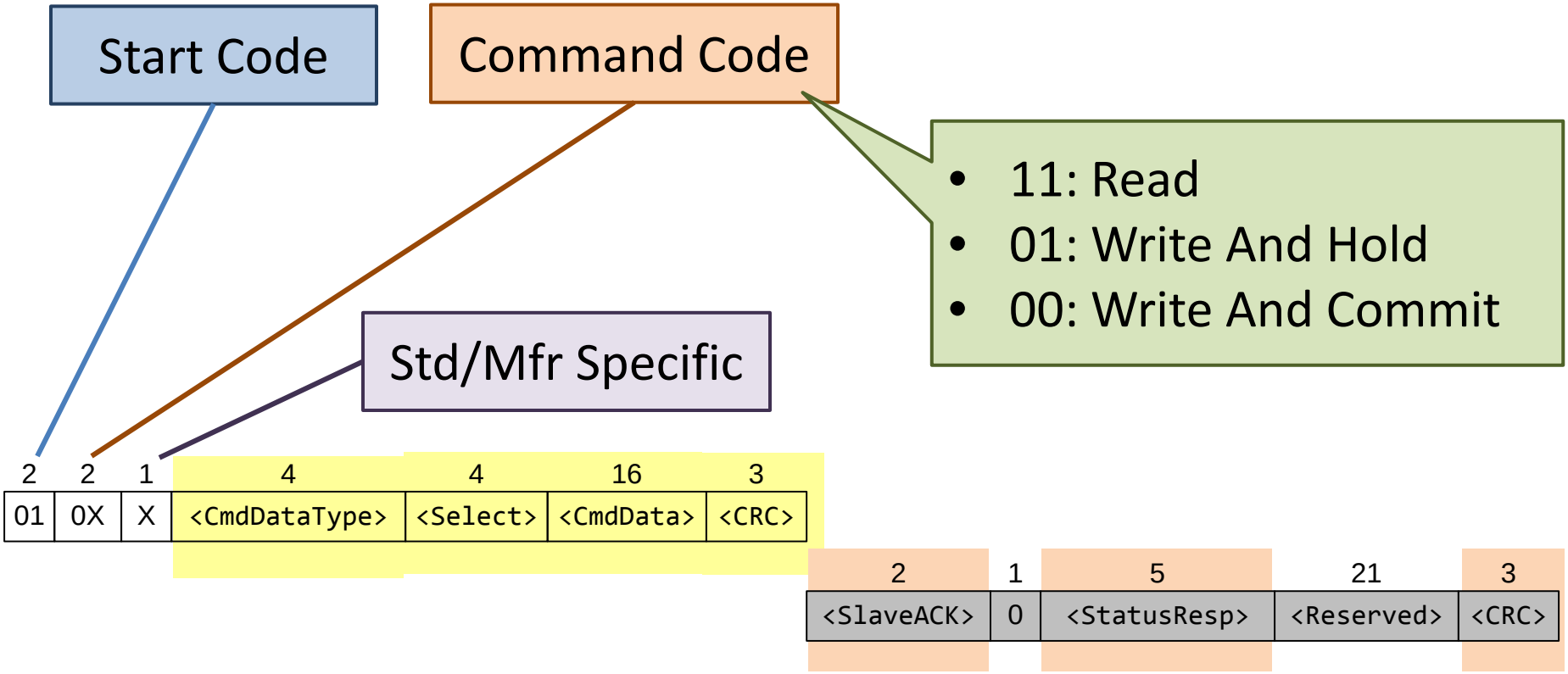


Response Frame From Slave To Master

The Write Frame

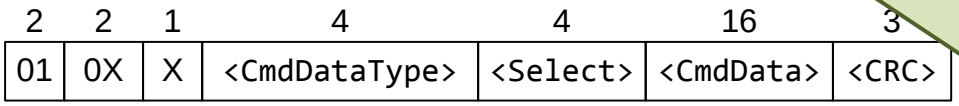


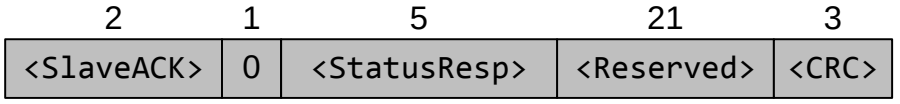
The Write Frame



Slave ACK

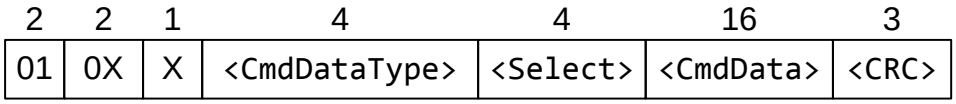
10: Bad CRC, No action taken
11: Good CRC, Invalid selector, No action taken
01: Good CRC but no action taken
because resource was unavailable
00: Good CRC, All OK and action taken

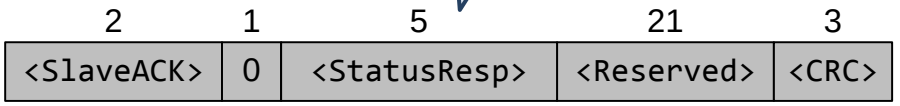




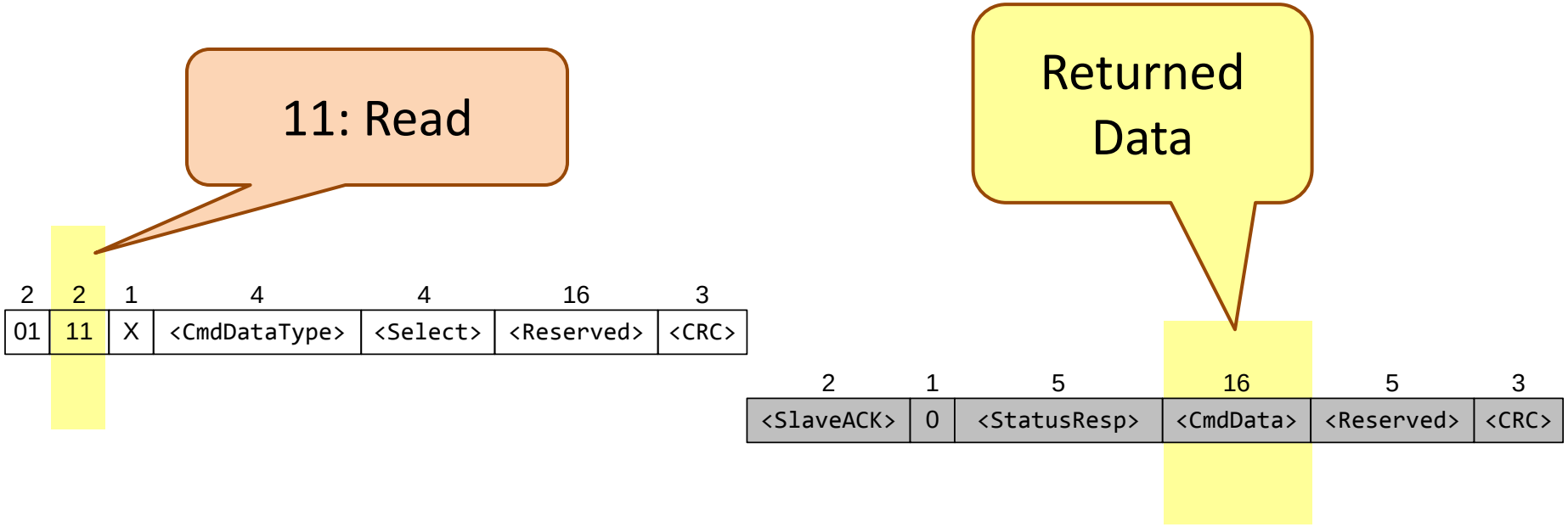
Status Response

- <VDone>
- <StatusAlert>
- <AVS_Control>
- <MfrSpcfc_Stts1>
- <MfrSpcfc_Stts2>

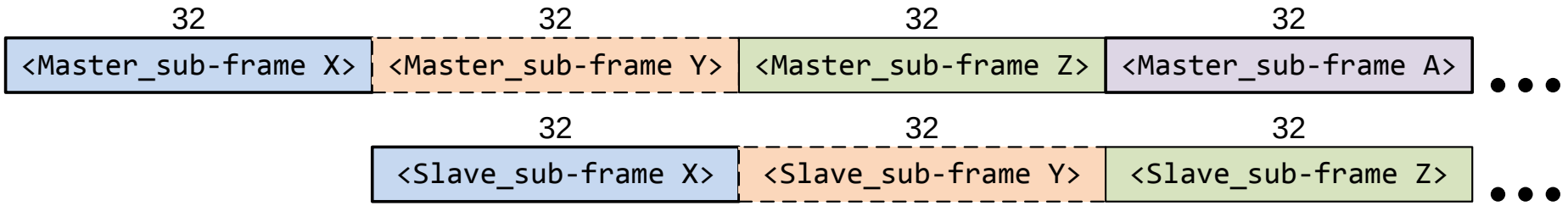




The Read Frame



Full Duplex Operation



Can Use This For A Multi-Rail Device
To Very Quickly Send Commands To All Rails

AVSBus Commands

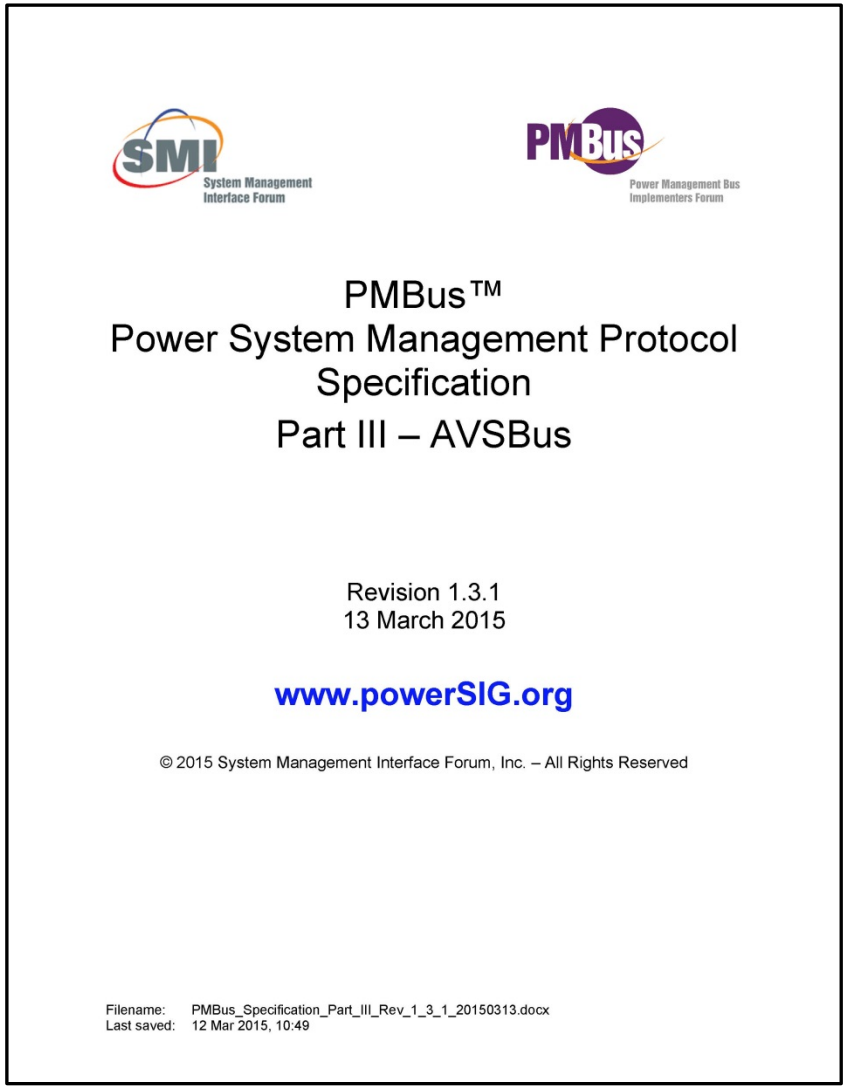
- Voltage Read/Write
  - 16 Bit Unsigned, 1 LSB = 1 mV
- Vout Transition Rate Read/Write
  - 16 Bit Unsigned, 1 LSB = 1 mV/µs
- Current Read
  - 16 Bit Unsigned, 1 LSB = 10 mA
- Temperature Read
  - 16 Bit Unsigned, 1 LSB = 0.1 °C

AVSBus Commands

- Voltage Reset
  - Emergency “Go To Default Value”
- Power Mode Read/Write
  - Maximum Power Or Maximum Efficiency
- AVSBus Status Read/Write
  - 5 Status Bits
- AVSBus Version Read
- Manufacturer Specific Read/Write

AVSBus Specification

- AVSBus Specification Is Part III Of The PMBus Specifications
- PMBus Specifications Available At www.pmbus.org
- No Cost
  - Registration Required



PMBus™
Power System Management Protocol Specification
Part III – AVSBus

Revision 1.3.1
13 March 2015

www.powerSIG.org

Filename: PMBus_Specification_Part_III_Rev_1_3_1_20150313.docx
Last saved: 12 Mar 2015, 10:49

AVSBus Credit

- AVSBus Concept And Draft Specification Originally Proposed To The PMBus Specification Working Group By:
  - Juan Arango, Texas Instruments
  - Travis Summerlin, Texas Instruments

AVSBus Summary

- Non-proprietary Serial VID
- Usable By Any Large Logic Device: Processor, ASIC, FPGA, …
- Task Focused, Not General Purpose
- Engineered For:
  - Speed
  - Simplicity
  - Low Cost

About The Presenter

Bob White has over 30 years experience in power electronics. He has held managerial and individual contributor positions in product development, technology development, applications and systems engineering, and technical marketing. His areas of expertise include power systems for computing and telecommunications systems, digital power, and applications of wide bandgap power semiconductor devices. Bob is currently the president and chief engineer of Embedded Power Labs, a power electronics consulting company.

Bob has been very active in the IEEE Power Electronics Society and the APEC committees, including twice serving as the APEC General Chair.

He is a Fellow of the IEEE, has a BSEE from MIT, a MSEE from Worcester Polytechnic Institute and is currently pursuing a Ph.D. in power electronics at the University of Colorado-Boulder. He is also an Honorably Discharged veteran of service in the United States Air Force.